CLAIMS

WHAT IS CLAIMED:

1. A method, comprising:

performing at least one electrical test on at least one semiconductor device;

determining at least one parameter of at least one process operation to be performed to form at least one gate insulation layer on a subsequently formed semiconductor device based upon electrical data obtained from said at lest one electrical test; and

performing said at least one process operation comprised of said determined at least one parameter to form said at least one gate insulation layer on said subsequently formed semiconductor device.

2. The method of claim 1, wherein said semiconductor device is at least one of a flash memory device, an application specific integrated circuit and a microprocessor.

3. The method of claim 1, wherein performing said at least one electrical test on said at least one semiconductor device comprises performing said at least one electrical test on said at least one semiconductor device to determine at least one of a breakdown voltage, a threshold voltage, a state charge, an interface charge, a trapped charge, a surface charge, a programming cycle time and an erase cycle time.

4. The method of claim 1, wherein said semiconductor device is comprised of at least one transistor that is comprised of a gate insulation layer and a gate electrode positioned above said gate insulation layer.

5. The method of claim 1, wherein said semiconductor device is comprised of a memory device that is comprised of a gate insulation layer, a floating gate layer positioned above said gate insulation layer, an intermediate insulation layer positioned above said floating gate layer, and a control gate layer positioned above said intermediate insulation layer.

6. The method of claim 1, wherein said at least one process operation is comprised of at least one of a deposition process and a thermal growth process.

7. The method of claim 1, wherein said at least one parameter is comprised of at least one of a temperature, a pressure, a duration, a process gas flow rate, a process gas composition, a liquid flow rate, a liquid composition, and a power level setting.

8. The method of claim 1, wherein said gate insulation layer is comprised of at least one of silicon dioxide and silicon nitride.

9. A method, comprising:

performing at least one electrical test on at least one memory device;

determining at least one parameter of at least one process operation to be performed to form at least one gate insulation layer on a subsequently formed memory device based upon electrical data obtained from said at lest one electrical test; and

performing said at least one process operation comprised of said determined at least one parameter to form said at least one gate insulation layer on said subsequently formed memory device.

10. The method of claim 9, wherein said memory device is a flash memory device.

11. The method of claim 9, wherein performing said at least one electrical test on said at least one memory device comprises performing said at least one electrical test on said at least one memory device to determine at least one of a breakdown voltage, a threshold voltage, a state charge, an interface charge, a trapped charge, a surface charge, a programming cycle time and an erase cycle time.

12. The method of claim 9, wherein said memory device is comprised of a gate insulation layer, a floating gate layer positioned above said gate insulation layer, an intermediate insulation layer positioned above said floating gate layer, and a control gate layer positioned above said intermediate insulation layer.

13. The method of claim 9, wherein said at least one process operation is comprised of at least one of a deposition process and a thermal growth process.

14. The method of claim 9, wherein said at least one parameter is comprised of at least one of a temperature, a pressure, a duration, a process gas flow rate, a process gas composition, a liquid flow rate, a liquid composition, and a power level setting.

15. The method of claim 9, wherein said gate insulation layer is comprised of at least one of silicon dioxide and silicon nitride.

16. A method, comprising:

performing at least one electrical test on at least one transistor;

determining at least one parameter of at least one process operation to be performed to form at least one gate insulation layer on a subsequently formed transistor based upon electrical data obtained from said at lest one electrical test; and

performing said at least one process operation comprised of said determined at least one parameter to form said at least one gate insulation layer on said subsequently formed transistor.

17. The method of claim 16, wherein performing said at least one electrical test on said at least one transistor comprises performing said at least one electrical test on said at least one transistor to determine at least one of a breakdown voltage, a threshold voltage, a state charge, an interface charge, a trapped charge and a surface charge.

18. The method of claim 16, wherein said at least one process operation is comprised of at least one of a deposition process and a thermal growth process.

19. The method of claim 16, wherein said at least one parameter is comprised of at least one of a temperature, a pressure, a duration, a process gas flow rate, a process gas composition, a liquid flow rate, a liquid composition, and a power level setting.

20. The method of claim 16, wherein said gate insulation layer is comprised of at least one of silicon dioxide and silicon nitride.

21. A method, comprising:

performing at least one electrical test on at least one memory device to determine a duration of a programming cycle performed on said memory device;

determining at least one parameter of at least one process operation to be performed to form at least one gate insulation layer on a subsequently formed memory device based upon said determined duration of said programming cycle; and

performing said at least one process operation comprised of said determined at least one parameter to form said at least one gate insulation layer on said subsequently formed memory device.

22. A method, comprising:

performing at least one electrical test on at least one memory device to determine a duration of an erase cycle performed on said memory device;

determining at least one parameter of at least one process operation to be performed to form at least one gate insulation layer on a subsequently formed memory device based upon said determined duration of said erase cycle; and

performing said at least one process operation comprised of said determined at least one parameter to form said at least one gate insulation layer on said subsequently formed memory device.